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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/578,362	01/16/2007	Stefan Tasch	00366.000210.	6884

5514 7590 01/07/2011

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EXAMINER	
WRIGHT, TUCKER J	

ART UNIT	PAPER NUMBER
2891	

MAIL DATE	DELIVERY MODE
01/07/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/578,362	TASCH ET AL.	
	Examiner	Art Unit	
	TUCKER WRIGHT	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26-53* is/are rejected.

7)☒ Claim(s) *43-44, 46* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/23/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/19/2010 has been entered.

Claim Objections

2. Claims 43, 44 and 46 are objected to because of the following informalities: "colour" should be "color." Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 47, 50 and 53 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,498,355 to Harrah.

Regarding claim 47, in FIG. 3, Harrah discloses a light-emitting diode chip (at least element 28); a multilayer board (6, 8, 10) having a base of a thermally well-conducting material (6; metal), the material including a metal, the base being

a core of the board (6 is the thickest board material) and configured for heat dissipation; and an electrically insulating (48) and thermally conducting connection layer between an emission surface of the light-emitting diode chip and the board, wherein between the light-emitting diode chip and the base of the board there is arranged an intermediate carrier (30/34) separate from parts with which the light-emitting diode chip is electrically contacted, and wherein the light-emitting diode chip is arranged on the intermediate carrier using a conductive adhesive (solder; col. 4, line 40).

Regarding claim 50, in FIG. 3, Harrah discloses that there is no electrically conducting layer between the intermediate carrier and the multi-layer board (a straight line can be drawn through a portion of intermediate carrier 30 and a portion of multi-layer board 10 that does not cross through any electrically conducting layers between the two).

Regarding claim 53, in FIG. 3, Harrah discloses that the electrically insulating and thermally conducting connection layer (48) is arranged between the intermediate carrier (30/34) and the base (6) of the board (6, 8, 10), whereby starting from the base of the board, the electrically insulating and thermally conducting connection layer is arranged above the base of the board, the intermediate carrier is arranged above the electrically insulating and thermally conducting connection layer, and the light emitting diode chip (28) is arranged above the intermediate carrier.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 26-28, 35, 38-41, 45, 48 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,498,355 to Harrah in view of US Patent No. 5,067,007 to Kanji.

Regarding claim 26, in FIG. 3, Harrah discloses a light-emitting diode chip (at least element 28); a multilayer board (6, 8, 10) having a base of a thermally well-conducting material (6; metal), the material including a metal, the base being a core of the board (6 is the thickest board material) and configured for heat dissipation; and an electrically insulating (48) and thermally conducting

connection layer between an emission surface of the light-emitting diode chip and the board, wherein between the light-emitting diode chip and the base of the board there is arranged an intermediate carrier (30/34) separate from parts with which the light-emitting diode chip is electrically contacted, wherein the intermediate carrier is formed of a ceramic material (col. 4, lines 38-40).

Harrah appears not to explicitly disclose that the ceramic intermediate carrier includes an aluminum nitride substrate.

Kanji discloses that aluminum nitride is a ceramic material (col. 5, lines 47-48).

To form a ceramic intermediate carrier, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a known ceramic material such as aluminum nitride.

Regarding claim 27, in FIG. 3, Harrah discloses that the electrically insulating connection layer is at least a boundary surface of the light-emitting diode chip (limitation defines the electrically insulating connection layer (48) as a boundary), which is arranged towards the board (faces board).

Regarding claim 28, in FIG. 3, Harrah discloses that the electrically insulating connection layer is at least an adhesive layer (layer 48 joins layers 46 and 30 and as such can be interpreted as an adhesive layer).

Regarding claim 35, in FIG. 3, Harrah discloses that the light-emitting diode chip is arranged so that the substrate of the light-emitting diode (bottommost surface of 28) is toward the board.

Regarding claim 38, in FIG. 3, Harrah discloses that the light-emitting diode chip is arranged so that a substrate of the light-emitting diode chip (bottommost surface of 28) is away from the board (28 is spaced apart from portions 6, 8, and 10 of board).

Regarding claim 39, in FIG. 3, Harrah discloses that the light-emitting diode chip is arranged on the intermediate carrier using a conductive adhesive (solder; col. 4, line 40).

Regarding claim 40, in FIG. 3, Harrah discloses that a side of the intermediate carrier towards the board is electrically insulating (portion 30 of the intermediate carrier is made of ceramic AlN).

Regarding claim 41, in FIG. 3, Harrah discloses that a region (34) of the intermediate carrier (30/34) towards the light-emitting diode chip has conductive regions (N-type contact is conductive).

Regarding claim 45, in FIG. 3, Harrah discloses that the light emitting diode chip (28) is connected to a circuit board (trace layer 8) using wires (48 and 50), and the circuit board is applied to the board (portion of board 6) using an insulating layer (10) positioned therebetween.

Regarding claim 48, in FIG. 3, Harrah discloses that there is no electrically conducting layer between the intermediate carrier and the multi-layer board (a straight line can be drawn through a portion of intermediate carrier 30 and a portion of multi-layer board 10 that does not cross through any electrically conducting layers between the two).

Regarding claim 51, in FIG. 3, Harrah discloses that the electrically insulating and thermally conducting connection layer (48) is arranged between the intermediate carrier (30/34) and the base (6) of the board (6, 8, 10), whereby starting from the base of the board, the electrically insulating and thermally conducting connection layer is arranged above the base of the board, the intermediate carrier is arranged above the electrically insulating and thermally conducting connection layer, and the light emitting diode chip (28) is arranged above the intermediate carrier.

7. Claims 46, 49 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,498,355 to Harrah in view of US Patent No. 6,682,331 to Peh.

Regarding claim 46, in FIG. 3, Harrah discloses a light-emitting diode chip (at least element 28); a multilayer board (6, 8, 10) having a base of a thermally well-conducting layer (6; metal), the layer including a metal, the base being a core of the board (6 is the thickest board material) and configured for heat dissipation; and an electrically insulating (48) and thermally conducting connection layer between an emission surface of the light-emitting diode chip

and the board, wherein between the light-emitting diode chip and the base of the board there is arranged an intermediate carrier (30/34) separate from parts with which the light-emitting diode chip is electrically contacted.

Harrah appears not to explicitly disclose a color conversion material that is arranged above and alongside the light-emitting diode chip.

In FIG. 1A, Peh discloses a similar device having a color conversion material (46) that is arranged above and alongside the light-emitting diode chip (40). The color conversion material allows a white solid-state lamp to be obtained from a conventional light-emitting diode (col. 1, lines 29-55).

To form a white solid-state lamp from a conventional light-emitting diode, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a color conversion material above and alongside the light-emitting diode chip.

Regarding claim 49, in FIG. 3, Harrah discloses that there is no electrically conducting layer between the intermediate carrier and the multi-layer board (a straight line can be drawn through a portion of intermediate carrier 30 and a portion of multi-layer board 10 that does not cross through any electrically conducting layers between the two).

Regarding claim 52, in FIG. 3, Harrah discloses that the electrically insulating and thermally conducting connection layer (48) is arranged between the intermediate carrier (30/34) and the base (6) of the board (6, 8, 10), whereby

starting from the base of the board, the electrically insulating and thermally conducting connection layer is arranged above the base of the board, the intermediate carrier is arranged above the electrically insulating and thermally conducting connection layer, and the light emitting diode chip (28) is arranged above the intermediate carrier.

8. Claims 29-34 and 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrah in view of Kanji as applied to claim 26 above, and further in view of US Pub. No. 2004/0065894 to Hashimoto.

Regarding claims 29 and 33, the combination of Harrah and Kanji appears not to explicitly disclose that the light-emitting diode chip is accommodated in a depression on the board.

In FIG. 11, Hashimoto discloses a similar device having a light-emitting diode chip (1) that is accommodated in a depression (11b) on a board (11). The sidewalls of the depression function as a reflector allowing for a more efficient extraction of the light emitted from the diode chip (see abstract).

To extract light from the diode chip more efficiently, it would have been obvious to one of ordinary skill in the art at the time the invention was made to accommodate the diode chip in a depression on the board.

Regarding claim 30, the combination of Harrah and Kanji appears not to explicitly disclose that the light-emitting diode chip is arranged in a region of a depression in the base material of the board.

In FIG. 11, Hashimoto discloses a similar device having a light-emitting diode chip (1) that is arranged in a region of a depression (11b) in the base material (11) of the board. The sidewalls of the depression function as a reflector allowing for a more efficient extraction of the light emitted from the diode chip (see abstract).

To extract light from the diode chip more efficiently, it would have been obvious to one of ordinary skill in the art at the time the invention was made to arrange the light-emitting diode chip in a region of a depression in the base material of the board.

Regarding claim 31, in FIG. 11, Hashimoto discloses that the light-emitting diode chip (1) does not project beyond a contour of the board (11).

Regarding claim 32, in FIG. 11, Hashimoto discloses that the light-emitting diode chip (1) ends flush (coplanar with) with an upper side of the board (uppermost surface of 11).

Regarding claim 34, in FIG. 11, Hashimoto discloses that the depression includes walls that are at least partially beveled.

Regarding claims 36 and 37, the combination of Harrah and Kanji is silent as to the structure of light-emitting diode chip (28) and as such appears not to explicitly disclose that the substrate of the light-emitting diode chip is formed of sapphire.

In paragraph [0003], Hashimoto discloses a light-emitting diode chip having a sapphire substrate and a gallium nitride light emitting portion on the sapphire substrate.

To form a working light-emitting diode arrangement, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a known light-emitting diode chip structure, such as that disclosed by Hashimoto.

9. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harrah in view of Kanji as applied to claim 26 above, and further in view of US Patent No. 5,512,131 to Kumar.

The combination of Harrah and Kanji discloses that the light-emitting diode chip is covered by a thick plano-convex lens (see element 26 in FIG. 3 of Harrah). As such, the combination of Harrah and Kanji appears not to explicitly disclose that the light-emitting diode chip is covered by Fresnel lens.

Kumar discloses that a Fresnel lens is a thin equivalent of a thick lens that is achieved by segmenting a spherical surface and moving each concentric segment toward the plano surface (col. 17, line 64 – col. 18, line 2). In other words, a Fresnel lens is a thinner, lighter lens with equivalent power to that of the thick lens.

To reduce the weight, thickness, and/or material used, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the thick plano-convex lens with a Fresnel lens.

10. Claims 43 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrah, Kanji and Kumar, and further in view of US Patent No. 6,682,331 to Peh.

Regarding claims 43 and 44, the combination of Harrah, Kanji and Kumar appears not to explicitly disclose that a region between the board and the lens is at least partially filled by a color conversion material, wherein the color conversion material is arranged above and alongside the light-emitting diode chip.

In FIG. 1A, Peh discloses a similar device having a region between the board (42) and the lens (50) that is at least partially filled by a color conversion material (46), wherein the color conversion material is arranged above and alongside the light-emitting diode chip (40). The color conversion material allows a white solid-state lamp to be obtained from a conventional light-emitting diode (col. 1, lines 29-55).

To form a white solid-state lamp from a conventional light-emitting diode, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a color conversion material above and alongside the light-emitting diode chip.

Response to Arguments

11. Applicant's arguments with respect to claims 26 and 46 have been considered but are moot in view of the new ground(s) of rejection.

12. Regarding claim 47, Applicant contends that "Harrah relies on solder bumps 32 and solder to connect LED 29 to submount 30, and does not rely on a conductive adhesive." (Applicant's 6/21/2010 Reply, pages 16-17)

This argument is not persuasive. As highlighted by Applicant, solder/solder bumps are used to connect LED 29 to submount 30. Solder is conductive and is used to physically attach LED 29 to submount 30. As such, solder/solder bumps are commensurate with "a conductive adhesive."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TUCKER WRIGHT whose telephone number is (571)270-3234. The examiner can normally be reached on Mon - Thur 8:30am-5:30pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kiesha Bryant can be reached on (571) 272-1844. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tucker Wright/
Examiner, Art Unit 2891